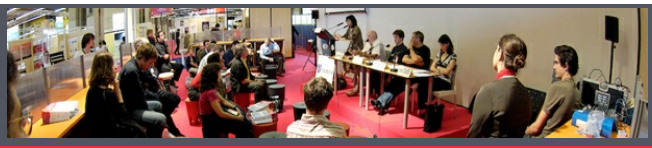
INTERNATIONAL RELATIONS



INTERNSHIP SUBJECT

2897 - Automated Design of Integrated Circuits with Open-Source Tools

Historically, the design and fabrication of Integrated Circuits (IC) has huge barriers of entry. Not only it requires highly technical knowledge, but also access to specialized software and confidential information from semiconductor manufacturers. In one hand, licenses for the mainstream Electronica Design Automation (EDA) tools can add up to a million dolars a year per workstation. In the other hand, the set of specifications of a certain fabrication technology, called a Process Design Kit (PDK), includes sensitive information, therefore, the manufacturer -or foundry- will tipically provide a PDK after signing a Non-Disclosure Agreement and pre-paying tens of thousands of dolars for the fabrication.

Since 2020, with the release of the first open-source PDK, these barriers have been greatly reduced. Along with recent improvements on open-source EDA tools (OpenRoad, Ngspice, KLayout, etc), open PDKs (sky130, gf180, ihp-sg13g2) have enabled fully free and open-source flows for IC design. In turn, this has also promoted research and development on automated design. Compared to digital systems, the analog flow is mostly manual, which means time-consuming and error-prone. Several frameworks based on open tools have been proposed to automate the design of analog and mixed-signal circuits. This is generally done by *programming* the design and physical implementation of a circuit, but specific solutions range from simple scripting to leveraging machine learning models.

You will start this internship by benchmarking these frameworks, considering completeness of the analog-mixed-signal (AMS) flow and performance of the automation features. The goal will then be to use the best one to extend previous work of the team and tackle the programmatic design of more and more complex circuits. The results will directly contribute to open knowledge on hardware design. In the long term, this work aims to accelerating the design of complete AMS systems, such as radio front-ends and processors for low-power microcontrollers, in association with collaborating teams.

If you like hardware design, building things and programming, this is the dream internship for you.

Work Environment

Located at the heart of Europe, Paris is a unique place to work and live in. Inria offers a unique balance between working in a leading research center, and living in one of the most beautiful and bustling cities in the world. A real communication hub, Paris is a gateway to France and Western Europe, and working in the Inria-Paris research center is real asset to your career. Inria Paris is located at the heart of the famous and picturesque Butte aux Cailles neighborhood in Paris.

Thanks to its top-quality researchers and numerous international guests, the Inria-Paris research center plays a leading role in international research, with a strong focus on networking, robotics and communication systems. The 32 research teams of the center are continuously pushing the boundaries in developing new concepts and techniques.

You will be working in a fantastically fun environment, within theAIO team (https://aio.inria.fr/), also in constant collaboration other international research teams, in particular Prof. Pister's team at UC Berkeley. The team is designing Tomorrow's Internet of (Important) Things. It pushes the limits of low-power wireless mesh networking by applying them to critical applications such as robotics, industrial control loops, with harsh reliability, scalability, security and energy constraints. Inria-AIO co-chairs the IETF LAKE standardization working group. Inria-AIO is heavily involved in real-world applications, and oversees over 1,000 sensors deployed on 3 continents for smart agriculture, smart city and environmental monitoring applications. The team's research program is organized around 5 pilars: Smart Dust, Low-Power Wireless Networking, Security in Constrained Systems, Swarm Robotics and Vehicle Area Networking.

Some pointers about the projects the AIO team is involved in:

- Team Homepage: https://aio.inria.fr/
- Thomas Watteyne's homepage: Thomas Watteyne

Required Skills

We are looking for a student pursing a Masters degree in Electronic Engineering or equivalent.

"hard" skills

- knowledge of analog and digital circuits and systems, ideally experience with SPICE simulation and hardware description.
- programming experience and skills (Python, C), ideally some experience with UNIX environments.
- project management tools (Git, GitHub, GitLab)
- ideally, hands-on prototyping experience (breadboard, FPGA, etc)

"soft" skils

- good communication skills and knowledge of English
- ideally, experience as a part of hardware/software development project or research team
- motivated and hard working

Communication within the team happens mostly in English, so speaking English is important. Speaking French is *not* a requirement, but a plus.

General Information

- **Research Theme :** Networks and Telecommunications
- **Locality :** Paris
- **Level :** Master
- **Period :** 1st January 2026 -> 31st March 2026 (3 months)

  These are approximative dates. Please contact the training supervisor to know the precise period.

- **Deadline to apply :** 1st July 2025 (midnight)

- Videos of things we have been doing: Videos, Videos
- mm-scale micro-electronics: Welcome! - SCuM - Confluence
- Falco spin-off startup company: Accueil - Falco
- Smart Agriculture deployment in Argentina: PEACH – predicting frost events in peach orchards
- Environmental deployment in California: SNOWHOW – Real-Time Real-World Monitoring Systems
- Smart city deployment in the French Riviera: Smartmarina – Innovation at Work
- open-source 6TiSCH implementation: Confluence

Contacts

- **Training Supervisor :** Alfonso Nicolas Cortes Neira / alfonso.cortes@inria.fr
- **Second Training Supervisor :** Vučinić Mališa / malisa.vucinic@inria.fr
- **Team Manager :** Malisa Vucinic / malisa.vucinic@inria.fr

More information

- **Inria Team :** AIO
- **Inria Center :** Centre Inria de Paris